PROCESS TECHNOLOGY AND MODELING OF A LOW-NOISE SILICON BIPOLAR TRANSISTOR WITH SUB-MICRON EMITTER WIDTHS

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Abstract

A low-noise silicon bipolar transistor with a 0.7 μm emitter width has been developed using a self-aligning process combined with ion implantation and local oxidation. Experimental noise figures of 1.45 dB at 1.5 GHz and 2.7 dB at 4 GHz are typical of transistor wafers made with this process. The best result obtained at 4 GHz was a noise figure of 2.3 dB with an associated gain of 9.5 dB. A T-equivalent circuit based on a regional analysis and empirical time constants is shown to accurately predict transistor S-parameters in the 1 to 8 GHz frequency range. Good agreement between predicted[3] and experimental amplifier noise figure is obtained between 0.4 and 6 GHz.

Introduction

The needs of many microwave radar and communication systems require front-end amplifiers with noise measures* as low as can be achieved by practical semiconductor devices. An example of such a device is the silicon bipolar transistor which has been found to be effective and reliable for low-noise applications in the 1 to 6 GHz frequency range. A significant improvement in the producibility, noise figure and associated gain of low-noise microwave bipolar transistors has been realized with the development of a totally ion implanted device with a 0.7 μm emitter width. With the use of empirically determined time constants, it will be shown that consistent noise figure and distributed equivalent circuit models are effective for predicting the noise performance and S-parameters of such transistors.

Design Approach

Any effective design for a low-noise microwave transistor will maximize available gain as well as minimize noise figure. A simple yet usefully accurate approximation for the maximum available transducer gain is

$$G_A(MAX) = \frac{f_T}{8\Pi r_b'(C_{CB} + C_{BP})f^2}$$

where f_T is the common emitter cutoff frequency, r_b' is the total base resistance, C_{CB} is the collector-base junction capacitance, C_{BP} is the collector base bonding pad capacitance and f is the operating frequency. $G_A(MAX)$ can be maximized for a particular emitter and base impurity profile, which determines f_T and r_b', by minimizing C_{CB} and C_{BP}. For modern low-noise transistors C_{CB} and C_{BP} are comparable. Within the limits of a particular technology, these capacitances can be made as small as possible by minimizing the center-to-center spacing between emitter strips and by maximizing the oxide thickness beneath the bonding pads.

The two major sources of noise in silicon bipolar transistors are thermal noise arising in the active and inactive base spreading resistances and shot noise due to the injection of current across the emitter-base junction. An optimized low-noise design will minimize the total base spreading resistance while simultaneously achieving a high f_T at a low-emitter current. Both of these objectives can be achieved by an interdigitated transistor design with emitter widths in the submicron range.

*Noise measure in dB is defined by $M = 10 \log 1 + \left[\frac{NF-1}{1-1/G_A}\right]$ which is the noise figure of an infinite chain of identical single stage amplifiers with noise figure NF and associated gain G_A.

Process

A process technology has been developed which allows the highly reproducible fabrication of a transistor with emitter-to-emitter spacings of 5 μm and emitter widths of approximately 0.7 μm by conventional contact lithography using hard-surface oxidized chrome photomasks. Transistors with this fine a geometry have previously been fabricated but usually with processes requiring projection mask aligners, electron-beam lithography or lateral diffusion techniques.

Two major features of the process are illustrated in the photomicrograph of Figure 1(a). The relatively thick oxide is formed by a local oxidation process that uses a silicon nitride cap to prevent the formation of oxide in the base region during a thermal oxidation cycle. This approach is used to eliminate the intolerable oxide steps that would result from conventional processes. The second major feature is the use of a self-aligning technique to simultaneously define the emitter and base contact windows in a silicon dioxide layer. The use of this self-aligning technique eliminates one of the most critical alignments and insures equal current injection from both sides of each emitter.

The photomicrograph of Figure 1(b) shows the completed transistor after the formation of the interdigitated metal pattern. The Ti/Pt/Au metal system is used in order to insure low contact resistance and excellent reliability.

S-Parameter and Noise Figure Models

White and Thurston[1] have developed the familiar lumped T-equivalent circuit for the modeling of the small-signal S-parameters of microwave transistors. This model has been refined by Kronquist et al[2] and shown to be satisfactory for accurately modeling the S-parameters of a 2.3 μm emitter width transistor at frequencies up to 4 GHz. We have found that basically this same equivalent circuit is also useful in modeling sub-micron emitter width low-noise transistors.

A cross-section of the active transistor region is shown in Figure 2. The lumped T-equivalent circuit shown in Figure 3 is based on a regional consideration of contact and spreading resistances and geometric cap-

acitances. The current dependent current source is driven by the current through the dynamic resistance of the forward biased emitter-base junction and the diffusion capacitance C_{DE}. The total common-base current gain α is approximated by the commonly used single pole expression

$$\alpha = \frac{\alpha_o \exp(-j2\pi f\tau)}{1 + j\, f/f_\alpha}$$

where f_α is the common-base cutoff frequency and τ is a delay time related the the base changing time τ_B and the collector region delay time τ_C. We assume that f_α is given by

$$f_\alpha = \frac{1}{2\pi\left(\tau_E + \frac{\tau_B}{1+m}\right)}$$

where τ_E is the emitter-base junction changing time, $R_{EO}C_{TE}$, and m is a constant. Measurements of $1/2\pi f_T$ as a function of $1/I_E$ are required to determine τ_E and τ_B. All other elements in the equivalent circuit are calculated from known process parameters. The constant m and the delay time τ are adjusted to maximize the agreement between modeled and experimental S-parameters. An independently determined equivalent circuit of the HPAC-70GT package is shown in Figure 4. The accuracy of the complete model is illustrated in Figures 5 and 6, which show the modeled and experimental values of $|S_{21}|^2$, $G_A(MAX)$, S_{11} and S_{22} as a function of frequency.

Using the expression derived by van der Ziel et al[3] we have modeled the frequency dependence of minimum amplifier noise figure. The same values for f_α and r_b' were used in the noise expression that were used in the S-parameter model. A comparison of typical measured noise figures and the model is given by Figure 7. The experimental values of associated gain are also shown.

Conclusions and Summary

A new process has been developed using ion implantation, local oxidation and self-aligning techniques. This process is ideally suited for the fabrication of discrete low-noise bipolar transistors with sub-micron emitter widths. A new transistor has been developed using this process that advances the state-of-the-art[4] for low-noise measure transistors designed for the 1 to 4 GHz frequency range. Typical experimental noise measures are 2.9 dB at 4 GHz and 1.5 dB at 1.5 GHz. A 2.3 noise figure with an associated gain of 9.5 dB was obtained at 4 GHz from the best unit. In addition to low minimim noise figure and high associated gain, this transistor is also characterized by a low equivalent noise resistance which allows near optimum performance over a large range of input match conditions. Both constant noise-figure and gain circles in the Γ_s plane at 4 GHz are shown in Figure 8 for a typical unit. It has also been shown that the regional T-equivalent circuit is useful for accurately modeling small-signal S-parameters and that the noise figure expression derived by van der Ziel et al[3] is sufficiently accurate to predict minimum noise figure in the 0.5 to 6 GHz frequency range.

Acknowledgements

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References

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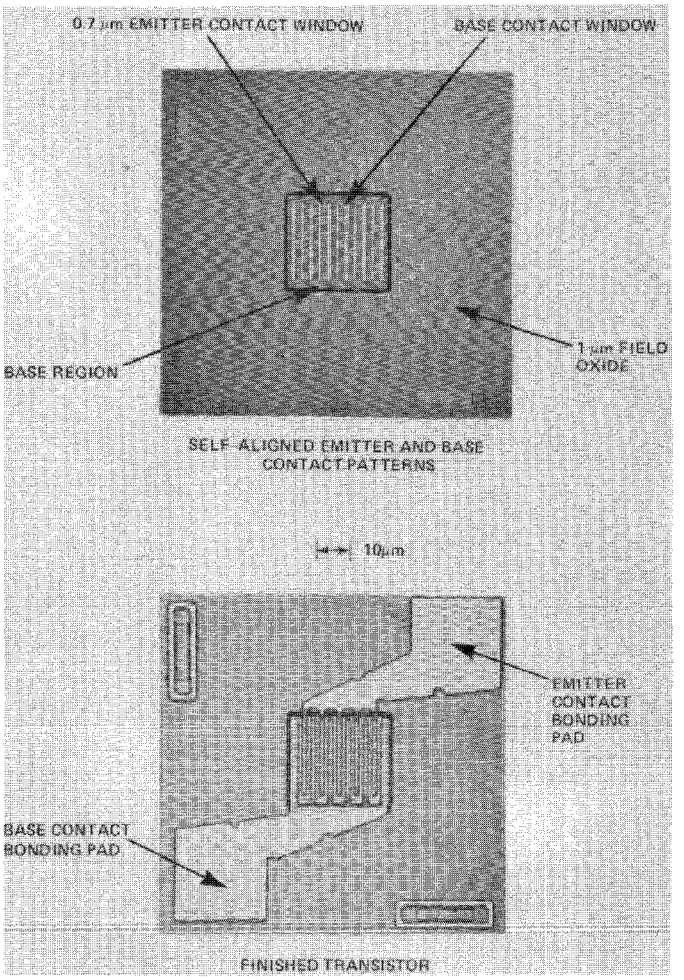

Fig. 1(a)-Photomicrograph of self-aligned emitter and base contact windows in central base region surrounded by local field oxide

(b)-Photomicrograph of finished transistor sans scratch protection

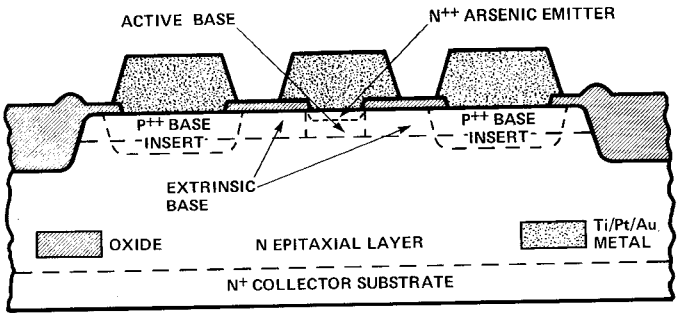

Fig. 2-Cross section of active transistor region through interdigitated emitter and base fingers

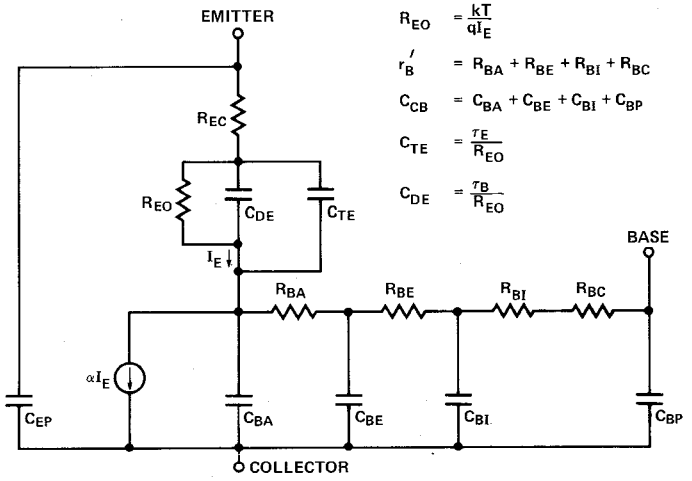

Fig. 3-Chip equivalent circuit

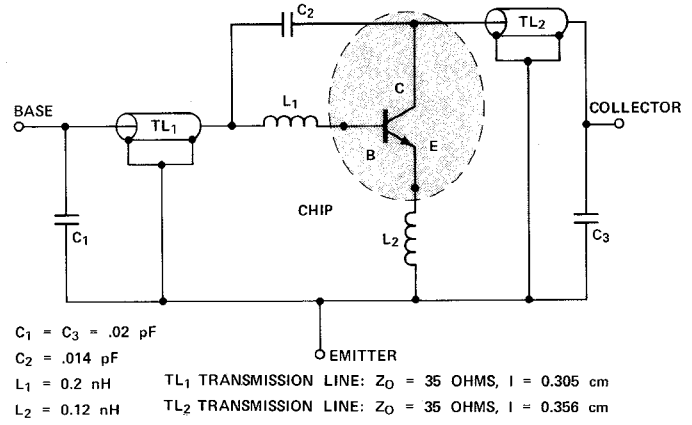

Fig. 4-Equivalent circuit of HPAC-70GT package

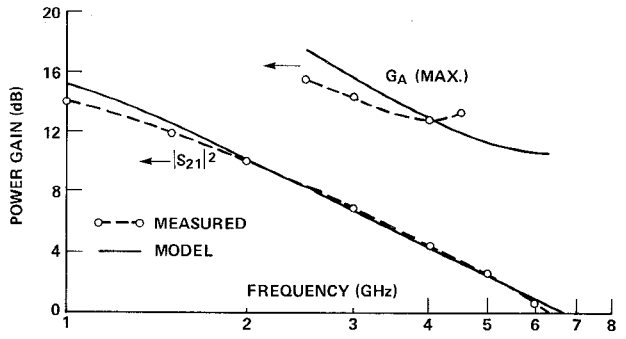

Fig. 5-Measured and modeled $|S_{21}|^2$ and G_A(MAX) gain of packaged device.

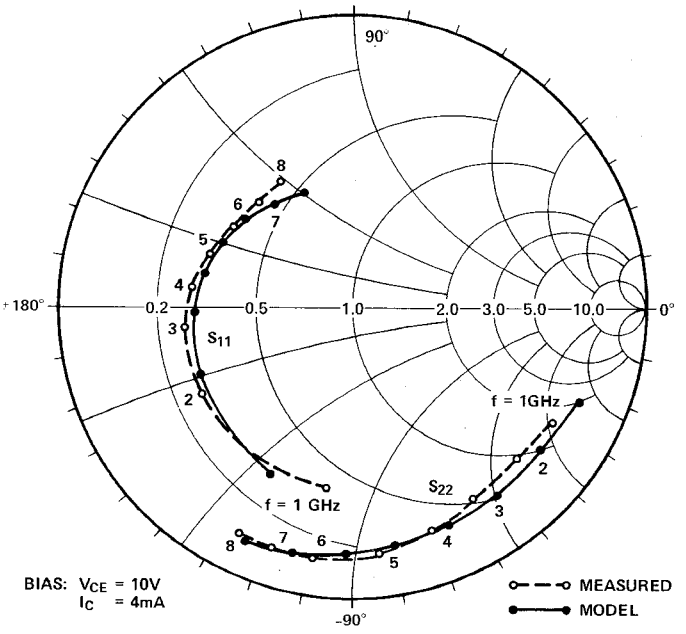

Fig. 6-Measured and modeled S_{11} and S_{22} of packaged devices

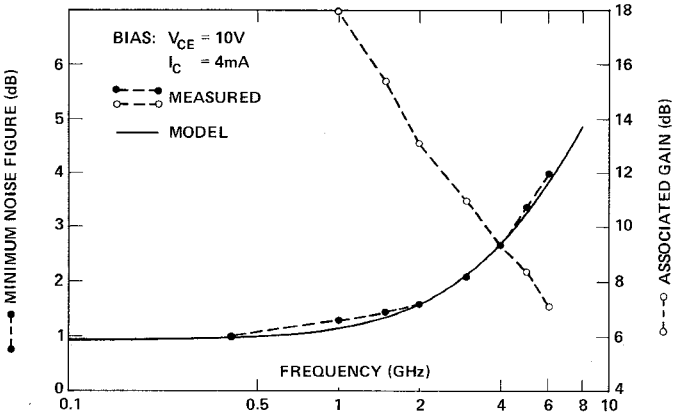

Fig. 7-Measured and modeled minimum noise figure.

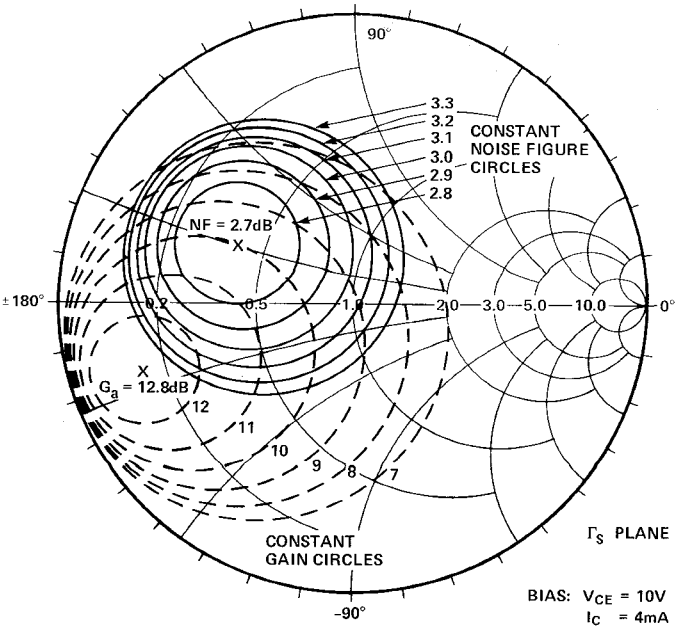

Fig. 8-Experimental constant gain and noise figure circles at 4 GHz